REMARKS

INTRODUCTION

Submitted herewith is a petition for one month extension of time. In the present response, without prejudice or surrender of any subject matter, claims 14, 28 and 36 have been canceled, and claims 1-13, 15-27, 29-35, 37-36, 51 and 52 have been amended. New claims have been added. Accordingly, claims 1-13, 15-27, 29-35 and 37-58 are no pending in the present application. The specification and abstract have been amended to correct matter of form and render them consistent with the claims. Support for these amendments is provided in Applicants' original disclosure (drawings and written description) and no new matter has been introduced by these amendments.

CLAIM OBJECTIONS

In the aforementioned Office Action, claims 1-56 have been objected to because of informalities. However, the claim amendments in this response render these objections moot. Accordingly, Applicants respectfully request withdrawal of the claim objections.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

Further in the aforementioned Office Action, claims 1-30 have been rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. However, the claim amendments in this response render these claim rejections moot and applicants request reconsideration and withdrawal of these claim rejections.

Claims 24-29, 34, 35 and 37-40 have also been rejected under 35 U.S.C. §112, 2nd paragraph. The rejected claims appear to the Examiner as being incomplete for omitting essential steps with such omission amounting to gap between the steps. Applicants respectfully disagree with this assessment. Nevertheless, because the claim amendments in this response render these claim rejections moot and because applicants believe that the claims as now presented comply with 35 U.S.C. §112, 2nd paragraph, Applicants respectfully request reconsideration and withdrawal of these claim rejections.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

Further in the aforementioned Office Action,

(i) claims 1-4, 6-12, 16, 18, and 23 have been rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent 5,900,834 to Kubinec in view of alleged knowledge in the art;

(ii) claim 5 has been rejected under 35 U.S.C. §103 as being unpatentable over Kubinec in view of U.S. Patent 6,304,116 to Yoon and further alleged knowledge in the art; and

(iii) claims 13, 14, 31, 31-33, 36 and 44 have been rejected under 35 U.S.C. §103 as being unpatentable over Kubinec in view of U.S. Patent 6,795,515 to Riedel and further alleged knowledge in the art.

However, applicants respectfully submit that the cited references do not support these claim rejections, singly or combined. First, the proposed combination of Kubinec and the alleged knowledge in the art about counters latching significant instances according to a master clock, over which claims 1-4, 6-12, 16, 18, and 23 have been rejected, does not produce the claimed invention as recited for instance in claim 1. Kubinec is directed to detection of a Doppler shift and even if combined with the alleged counters latching significant instances in accordance to the master clock it fails to produce jitter measurement as provided in the claimed invention. In other words, as hereafter shown, Kubniec does not teach each and every element of this claimed invention, and the alleged knowledge in the art about counters doesn't make up for the deficiencies in Kubinec.

Specifically, claim 1 is directed to a circuit for measuring jitter which comprises:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal, the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage element any pulse that is active at the time of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality of trigger signals has occurred.

At the same time, Kubinec discloses a Doppler shift detector that uses clocked delay lines for determining the Doppler shift between a transmit signal and a receive signal (e.g., Abstract). The Doppler shift detector is disclosed as having a delay line, a periodic detection logic and a Doppler shift detector (See, e.g., Fig. 1(a)). In the delay line, with the plurality of delay stages propagating a signal and signal detection logic coupled to selected ones of the delay stages, the signal detection logic produces a signal indicative of an edge of the signal at selected delay stages (see, e.g., Fig. 3(a), col. 6, lines 26-55, col. 7, lines 9-35 and claim 1). Further in the delay line, a plurality of counters are coupled to the signal detection logic and are connected to receive a common clock signal for counting a number of signal edges at the selected delay stages. *Id.* The period detection logic is coupled to the delay line for inspecting the counter values of the detected edges to determine the period of the applied transmit signal (see. e.g., col. 4, lines 6-14 and claim 1).

Note that the presence of jitter is exploited in Kubinec's circuit to obtain measurement of the mean position (tap point in the chain) of the detected edges (see, e.g., col. 4, lines 21-32). According to Kubinec, this mean position is expressed as a fractional number of delay stages (tap points). Thus, the jitter is averaged away to find the average of the tap point number for the delay stages that have detected edges, weighted by the number of detected edges counted for each delay stage (See, e.g., Col. 4, lines 14-25). Moreover, the delays in Kubinec' circuit are not arbitrary, but in fact necessarily equal to each other in order to accurately measure the period of the transmit signal (see, "common delay period," col. 4, lines 49-64, col. 6, lines 10-24, and "uniform delay," col. 7, lines 9-20). The uniform delay period provided by each of the delay stages is synchronized to a reference clock period according to a calibration signal (see, col. 7, lines 1-20).

Then, the multi-bit signal at the output of the periodic detection logic indicates the respective periods of the transmit and receive signals (See, col. 4, lines 65-67). The Doppler shift detector calculates the difference in frequencies between the transmit and receive signals, i.e., it calculates the Doppler shift (see, e.g., Fig. 1(a) and claim 1).

Thus, although Kubinec exploits the presence of jitter to obtain measurement of the mean position, it does not proceed to provide jitter measurement like the circuit of claim 1. Indeed, unlike the circuit of claim 1, Kubinec's circuit uses a common (uniform) delay period in order to obtain an accurate frequency measurements with which it proceeds to measure the period of the transmit and receive signals so that they can be compared to find the Doppler shift. In contrast, the circuit of the present invention as recited in claim 1 does not need to have common (uniform) delays as it does not measure the period of a signal. Rather, the circuit of the present invention measures the shift in position of a significant instant of the clock signal over many samples to find the jitter of the significant instant of the clock signal.

Furthermore, while in the circuit of claim 1 there is "a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage element any pulse that is active at the time of occurrence of the trigger signal," by contrast, the plurality of counters in Kubniec's circuit are coupled to the signal detection logic and are connected to receive a common clock signal for counting a number of signal edges at the selected delay stages. Indeed, there is no mention in Kubinec of the trigger timing for example where there is "a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain." Finally, while Kubinec produces the Doppler shift, by contrast, the circuit of claim 1 produces jitter measurement "wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality trigger signals has occurred."

Accordingly, Kubinec does not teach or suggest a circuit as recited in claim 1, even in combination with the aforementioned alleged knowledge in the art about

counters. In fact, the alleged knowledge in the art on which the Examiner relies, a comparison between storage elements and counters, even if it were to be relevant or correct, does not make up for Kubinec's deficiency in failing to produce the claimed circuit as recited in claim 1. Additionally, such proposed combination would not operate as originally intended by the present invention as recited in claim 1.

For these and other reasons, the claims that depend from claim 1 are distinguishable from Kubinec in combination with the alleged knowledge about counters. For instance, Kubinec does not teach that N, the number of delay elements recited in claim 3, "is an even number greater than 2 and implemented as a power of 2."

Next, as to claim 5 which also depends from claim 1, the Examiner proposes a combination of Kubinec, Yoon and alleged knowledge in the art about voltage controlled delay lines to produce the claimed invention. Yoon discloses delay locked loop circuits, phase detectors and methods for producing a delayed signal from a periodic input signal. In particular, the delay locked loop in Yoon includes a delay line with a series-connected chain of delay units, a phase detector and a charge pump (see, e.g., Fig. 4 and col. 5, line 45 to col. 6, line 43). The phase detector received delayed signals from the output and middle of the delay line and an input signal and it is configured to detect a difference in phases between these signals. The charge pump generates a delay control voltage that varies (reduces/increases) the delay in response to the phase comparisons. *Id.*

Thus, the combination of Kubinec and Yoon produces Doppler shift measurement with delay locked loops for detecting phase shifts and controlling the delay elements' delay. Combined also with the alleged knowledge in the art about voltage controlled delay lines, together, the teachings of Kubinec and Yoon do not produce the present invention as recited in claim 5. In particular, in this combination Kubinec does not teach that at least one of the plurality of associated delays is not equal to any other of the plurality of associated delays, and Yoon along or with the alleged knowledge about voltage controlled delay lines does not make up for this deficiency. Moreover, the combination of Kubinec and Yoon would not have operated as originally intended for the circuit of claim 5, and there would not have been motivation to combine Kubinec and Yoon because Yoon and Kubinec are not in the same field of endeavor as demonstrated

by the fact they do not belong in the same classification (Kubinec is in PTO class 342/115 and Yoon is in PTO class 327/158).

As to claim 13 (14 is cancelled), the proposed combination of Kubinec with Riedle and alleged knowledge about master clocks generating a trigger signal to latch an output of an edge detector into memory, over which claim 13 is rejected, fails to produce the claimed invention. In particular, Riedle discloses a circuit for optimizing the sampling time for sampling bits in a serial data stream (see, e.g., Fig. 2). The circuit includes a delay line with a plurality of delay elements having a delay, say, 400ps, where each delay element output in the line is a sampling position having a unique time position with respect to the stored data (see, e.g., col. 3, lines 1-21). The delay sampling positions are predetermined based on initialization bits (see, "training procedure," col. 4, lines 11-15), and based on multiple delay line samples, detecting data bit edges along the line, delay line sample edge masks are produced (col. 4, lines 18-37). Once the delay line sample masks are generated, they can be analyzed to determine where adjacent bits exit and thereby determine an optimal sampling point for each of the adjacent bits (col. 4, lines 53-60). Riedle discloses also that accurate sampling of the data, which is subject to jitter, requires selection of sampling position on the delay line that is least susceptible to the effects of jitter. To this end, the sampling positions are determined initially during the training process and then they are updated during data reception (col. 3, lines 19-65). Appropriate sample times are provided in order to select sampling from the appropriate positions, and these sample times correspond to an optimum sample position in the delay line for sampling the two adjacent bits (Fig. 2 and col. 3, lines 62-67). The processor controls this timing (col. 3, lines 62-67).

Thus, the combination of Kubinec and Reidle produces Doppler shift measurement and determination of optimal sampling positions on the delay line with sampling timing determined for optimal sampling positions. However, even with alleged knowledge in the art about latch timing, this combination does not teach or suggest that "the trigger signal is delayed by a first predetermined delay from the reference signal," because the timing discussed in Riedle (Fig. 2) applies to the "MUX1_SEL 0:4" and "MUX2_SEL 0:4" signals to select one of the 32X1MUXs rather than the "4ns b_clock" signal to the L2 latches. By contrast, in the circuit of the present invention as recited in

claim 13, the trigger signal, which is delayed by a predetermined delay from a reference clock, is applied to record the pulses in the storage elements of the second circuitry. In other words, the predetermined time delay of the trigger signal to the storage elements in claim 13 is not the same as the timing of the select signals to the MUXs. Therefore, the combined teachings of Kubinec, Riedle and alleged knowledge about latch timing do not produce the claimed invention as recited in claim 13.

Moreover, Riedle is not properly combined with Kubinec because they are in different fields of endeavor. In fact, Riedles' method of locating sampling points in a synchronous data stream is in a different field of endeavor relative to Kubinec's Doppler shift measurement, nor is Riedle pertinent to the practice of the present invention, and a person of ordinary skill in the art would not be motivated to combine Reidle's teaching with Kubinec to produce the claimed invention (Reidle PTO class 375/355, Kubinec PTO class 342/115).

As to claim 31, the examiner relies on Kubinec, Riedle and alleged knowledge about latch time, but these references fail to teach or suggest the claimed method, singly or in combination. In other words, as hereafter shown, the combination of Kubinec's Doppler shift detection, Riedle's process for locating sampling points and the alleged knowledge about latch time fails to have each and every element of the method for measuring jitter as recited in claim 31. This method includes:

> for each of a plurality of trigger signal occurrences, performing the steps of
>
> receiving the clock signal, the clock signal having a significant instant;
>
> propagating the significant instant of the clock signal through a chain of delay elements, wherein each element has an associated delay and the chain has a total delay equal to the sum of the associated delays;
>
> receiving a trigger signal and delaying the received trigger signal to occur at a time equal to approximately have the total delay of the chain;
>
> detecting propagation of the significant instant of the clock signal through each of the delay elements in the chain and producing a pulse corresponding thereto;
>
> recording any pulse that is coincident with the trigger signal; and
>
> producing a jitter measurement signal responsive to the

recorded pulses after the plurality of trigger signal occurrences.

While Kubinec's circuit introduces an input signal to its delay stages and a common clock to its counters, unlike the claimed method, Kubinec does not introduce "receiving a trigger signal and delaying the received trigger signal to occur at a time equal to approximately have the total delay of the chain." Also, while the circuit in Kubinec counts signal edges in select stages and produces a Doppler shift therefrom, unlike the method of claim 31, Kubinec does not teach or suggest "performing the steps recited above for each of a plurality of trigger signal occurrences."

Moreover, Riedle and the alleged knowledge about latch times do not fill in the gap left by Kubinec. They do not teach or suggest "receiving a trigger signal and delaying the received trigger signal to occur at a time equal to approximately half the total delay of the chain."

For these as well as other reasons, the claims depending from claim 31 are also distinguishable from Kubinec, Riedle and the alleged knowledge in the art, singly or combined. For instance, claim 32 recites "deriving a jitter measure through a comparison of the jitter measurement signal to an associated delay." Kubinec does not teach this feature nor does Riedle, and combined they do not produce the method of claim 32. In another example, Claims 33-35 recite "filtered jitter..." and none of this is disclosed or suggested by Kubinec or Riedle.

In view of the forgoing, Applicants respectfully submit that the claimed invention as recited in claims 1-13, 15-27, 29-40 and 44 is neither taught nor suggested by the cited references. As a result, Applicants believe that above-enumerated claims, 1-13, 15-27, 29-40 and 44, are allowable over the cited references and respectfully request reconsideration and withdrawal of the claim rejections in view of these references.

ALLOWABLE SUBJECT MATTER

Applicants acknowledge and appreciate the indication of allowable subject matter. Although, as outlined above, Applicants believe that the subject matter in claims 1, 31 and their respective dependent claims are also allowable, applicants agree that claims 41-

43 and 45-56 are also allowable over the cited references which fail to teach, for example, the response to jitter measurements.

NEW CLAIMS

Claims 57 and 58 have been added to further point out aspects of the invention. Claims 57 and 58 are allowable over the cited references for similar reasons as stated above.

CONCLUSION

Having addressed each and every ground of objection and rejection, applicants believe that the application is in condition for allowance. Applicants respectfully request reconsideration and allowance of the pending claims in the above-mentioned application and respectfully request that a timely Notice of Allowance be issued in this case.

The examiner is authorized to charge any fee deficiency or credit any fee overpayment to Deposit Account 50-2778.

Respectfully submitted,

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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited on July 19, 2005, with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450.

Date: July 19, 2005

Yolette Ytuzalde-Owen